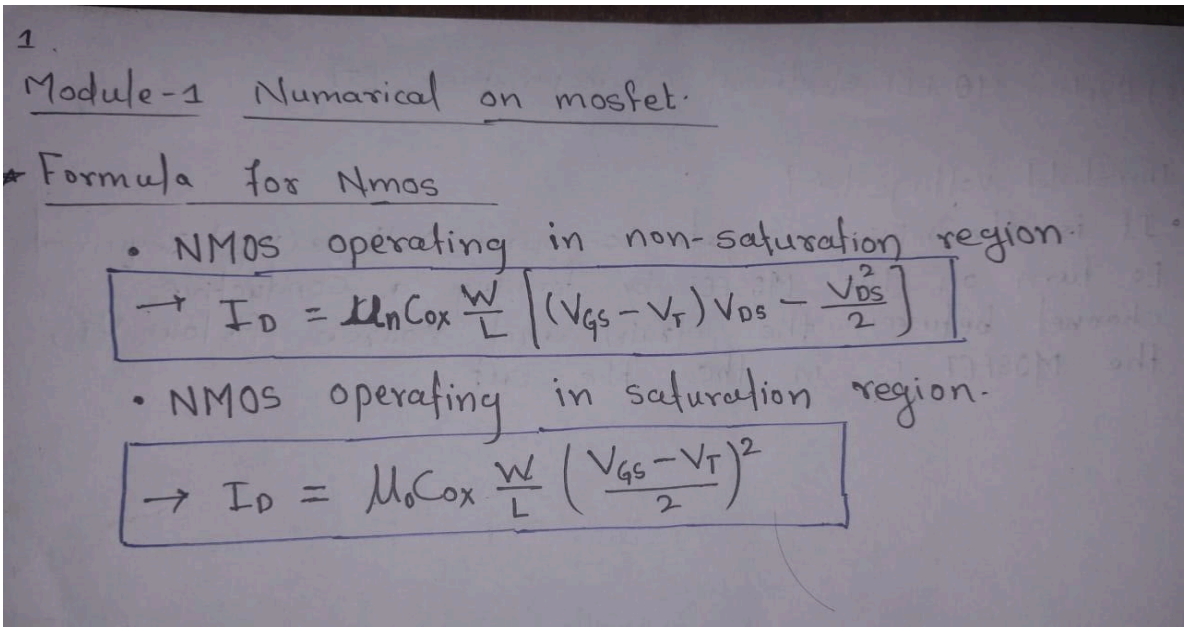
Module 1

Q1) For n-channel MOSFET VT = 1.75 V, VGS=5V, VDS = 2V, ID = 120A, COX=51.72 nF/CM2, μn =400 CM2/S. Find the region of operation and W/L ratio



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Q2) Explain MOSFET electrical characteristics

MOSFET Electrical Characteristics:

1. **Threshold Voltage (V_T):**
   - It is the minimum gate-to-source voltage (V_{GS}) required to turn on the MOSFET by forming a conductive channel between the drain and source. Below V_T, the MOSFET is in the **cutoff region** (OFF state) and no current flows.
   - For an **n-channel MOSFET**, V_T is positive, while for a **p-channel MOSFET**, V_T is negative.
2. **Drain Current (I_D):**
   - The current flowing from drain to source depends on the operating region:
     - **Cutoff Region:** $I_D = 0$ when $V_{GS} < V_T$.
     - **Linear (Ohmic) Region:** The MOSFET acts like a variable resistor; current depends linearly on V_{DS}.
     - **Saturation Region:** I_D becomes independent of V_{DS} and depends on V_{GS} according to the equation $I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2$.
3. **Transconductance (g_m):**
   - It measures the sensitivity of the drain current to the gate voltage. It is defined as $g_m = \frac{\partial I_D}{\partial V_{GS}}$ and reflects how effectively the MOSFET controls the current flow through the channel.
4. **Channel Length Modulation:**
   - In the **saturation region**, even though the current ideally remains constant, the length of the channel decreases as V_{DS} increases, causing a small increase in I_D. This is represented by the factor $(1 + \lambda V_{DS})$, where λ is the channel-length modulation parameter.

5. **Capacitances:**
   - MOSFETs have internal capacitances that affect their switching behavior, especially in high-speed applications:
     - **Gate-to-Source Capacitance** (C_{gs}),
     - **Gate-to-Drain Capacitance** (C_{gd}) (Miller capacitance),
     - **Drain-to-Bulk Capacitance** (C_{db}).

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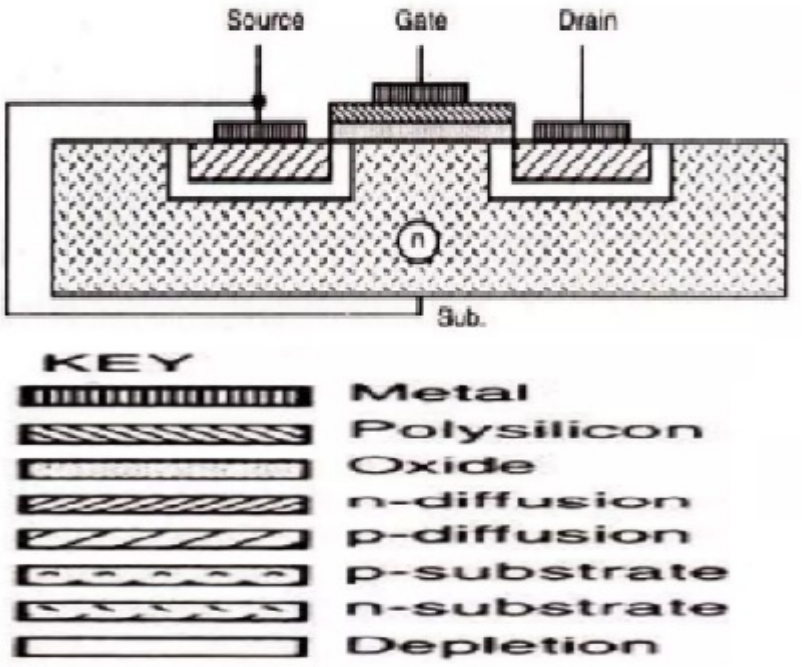
Q3) Explain P-MOS fabrication with a neat and clean diagram.



P-MOS (P-type Metal-Oxide-Semiconductor) transistors are key components in many modern electronic devices. The process of fabricating a P-MOS transistor involves several steps, each of which is crucial to creating the final structure. Below, I'll explain the steps involved in the fabrication of a P-MOS transistor along with a description of the structure, and I will generate a diagram to visually explain it.

Steps in P-MOS Fabrication Process

1. **Starting Substrate**:
   The fabrication begins with an N-type silicon wafer, which serves as the base material. The N-type silicon has an abundance of electrons.
2. **Oxidation**:
   A thin layer of silicon dioxide (SiO_2) is grown on the surface of the wafer using thermal oxidation. This layer acts as an insulator and is used for the gate oxide in the transistor.
3. **Photolithography and Etching**:
   Photolithography is used to pattern the silicon dioxide layer. A photoresist material is applied to the wafer and exposed to UV light through a mask that defines the regions where the oxide needs to be etched away. After exposure,

the unprotected areas are etched away, exposing the underlying N-type silicon.

4. **P-Well Formation**:
   In the exposed areas of the N-type silicon, P-type impurities (such as boron) are implanted using ion implantation or diffusion. This creates the P-well region, where the P-MOS transistor will be built.
5. **Gate Oxide Formation**:
   A thin gate oxide layer is grown again in the P-well region. This oxide will act as the insulator between the gate and the channel of the MOSFET.
6. **Polysilicon Deposition**:
   A layer of polysilicon is deposited on top of the wafer, which will later serve as the gate material. The polysilicon layer is patterned and etched to form the gate electrode.
7. **Source and Drain Formation**:
   After the gate is defined, more P-type dopants are implanted into the areas on either side of the gate. These areas will become the source and drain of the P-MOS transistor. The gate helps to define the exact region where the channel will form between the source and drain.
8. **Metal Contacts**:
   Finally, metal contacts are deposited and patterned to connect to the source, drain, and gate regions. This provides electrical access to the transistor.
9. **Passivation Layer**:
   A protective passivation layer is deposited over the entire surface of the chip, with openings made for the metal contacts. This layer protects the device from contamination and mechanical damage.

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Q4) Explain short channel effects in VLSI.

Short channel effects happen when the channel length of a MOSFET becomes very small, almost equal to the depletion region widths of the source and drain. This causes certain unwanted effects.

Main Effects:

1. **Drain-Induced Barrier Lowering (DIBL):**
   When drain voltage increases, it lowers the barrier in the channel, making it easier for electrons to flow from source to drain, even if the gate voltage is less than the threshold voltage.

2. **Velocity Saturation:**
   As the channel length becomes shorter, electrons move at a maximum speed, limiting the current, no matter how much you increase the voltage.
3. **Hot Carrier Degradation:**
   High-energy electrons damage the MOSFET material over time, reducing its lifespan.
4. **Impact Ionisation:**
   High-energy electrons collide with atoms, creating extra current, which is undesirable.
5. **Surface Scattering:**
   In short channels, electrons bounce off the channel surface, slowing them down and reducing current.

Why DIBL is Important:

In short-channel devices, the source and drain get closer, and their electric fields start to interfere. This allows the drain to influence the potential barrier at the source, making it easier for electrons to flow even when the gate voltage is lower than needed (DIBL effect).

How to Avoid Short Channel Effects:

- **New MOSFET Designs**: Use FinFETs or Nanowires.
- **SoT Technology**: Spin-Orbit Torque.
- **High-k Dielectric Materials**: Reduce leakage current.
- **Use Compound III-V Materials**: These materials have better properties for reducing short channel effects.

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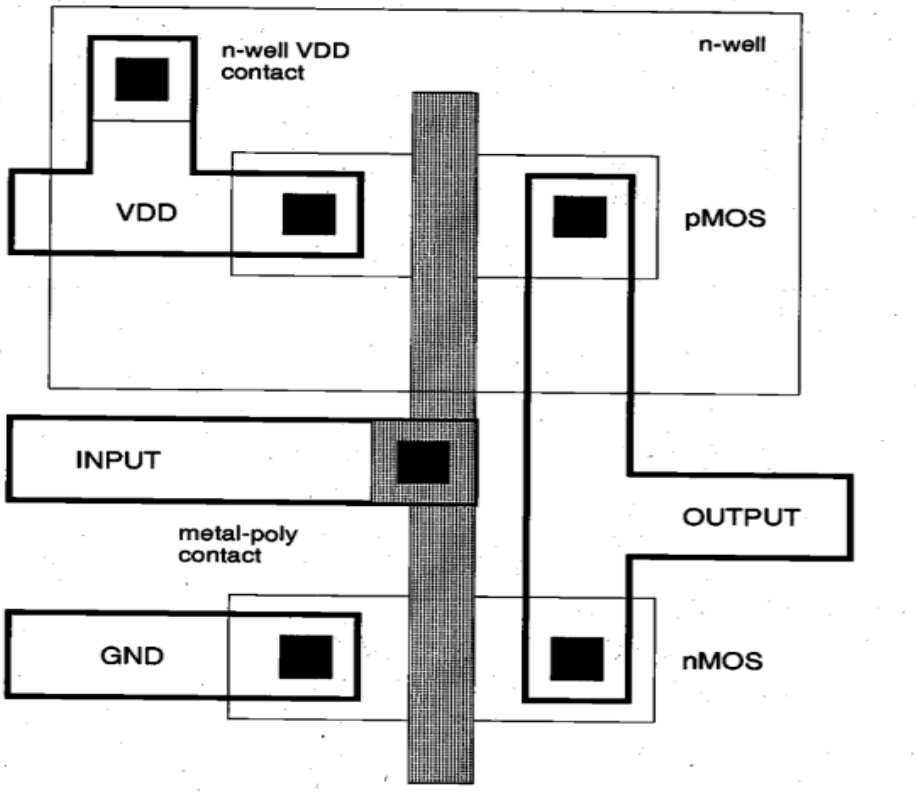
Q6) Draw layout of Inverter using lambda based design rules



Lambda (λ) is a design parameter used to scale CMOS circuits. Here's a straightforward way to understand it:

What is Lambda (λ)?

- **Definition:** Lambda (λ) is a reference length used in IC design to standardize and scale design rules. It simplifies the process of adjusting design dimensions as technology shrinks.

How It Works:

1. **Design Rules:**
    - Design rules (like minimum widths, spacing) are expressed as multiples of λ. For example, if λ = 0.5 µm, then a minimum gate width of 2λ is 1 µm.
2. **Scaling:**
    - As technology improves, λ decreases. All design dimensions are scaled down proportionally. For instance, if λ changes from 0.5 µm to 0.25 µm, the design dimensions (like gate width) are halved.

Why Use Lambda-Based Design?

- **Consistency:** Ensures uniformity in design rules across different technology nodes.
- **Simplicity:** Simplifies the process of designing and scaling ICs by using a single parameter for all dimensions.

Example:

- **λ = 0.5 µm:** If a gate width is specified as 3λ, it equals 1.5 µm.
- **λ = 0.25 µm:** The same gate width of 3λ would now be 0.75 µm.

Diagram:

Here's a simple visual to help you remember:

```scss
+----------------------+
|       Lambda (λ)     |
|                      |
|  λ = 0.5 µm          |
|  Gate Width = 3λ     |
|  => 1.5 µm           |
|                      |
|  Technology Shrinks  |
|  λ = 0.25 µm         |
|  Gate Width = 3λ     |
|  => 0.75 µm          |
+----------------------+
```

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Q7)Explain nMOS fabrication process with neat and clean diagrams

nMOS Fabrication Process

1. **Start with Silicon Wafer:**
    - Begin with a **p-type silicon wafer**. Grow a thick layer of **silicon dioxide (SiO_2)** on it. This layer is called the **field oxide** and is used to isolate individual transistors.
2. **Pattern the Field Oxide:**
    - Use a **photolithography process** to selectively etch away the field oxide, exposing the silicon surface where the MOS transistor will be made. This process defines the areas for the transistors.
3. **Grow Thin Oxide Layer:**

    - Grow a thin layer of silicon dioxide (called **thin oxide or thinox**) over the entire surface of the wafer. On top of this, deposit a layer of **polysilicon** (a type of silicon used for the gate).
4. **Pattern the Gate:**
    - Use photolithography to **etch away** parts of the polysilicon layer to form the **transistor gate**. This process is known as the **self-aligned process** because the source and drain regions will be correctly aligned under the gate.
5. **Remove Exposed Gate Oxide:**
    - Remove any exposed **gate oxide** that was not covered by the polysilicon gate. This step prepares the wafer for doping.
6. **Dopant Implantation:**
    - Expose the wafer to a **dopant source** or use **ion implantation** to create the **source and drain regions**. This also helps in reducing the resistivity of the polysilicon gate.
7. **Add Contacts:**
    - Cover the entire wafer with **SiO_2** again. **Etch contact holes** in the SiO_2 layer to connect the source and drain regions to the outside world.
8. **Metal Layer:**
    - Finally, deposit a **metal layer** (usually aluminum) and **pattern** it to create the **interconnects** that connect the transistor to other parts of the circuit.

gions are formed only in the region where | interconnects.

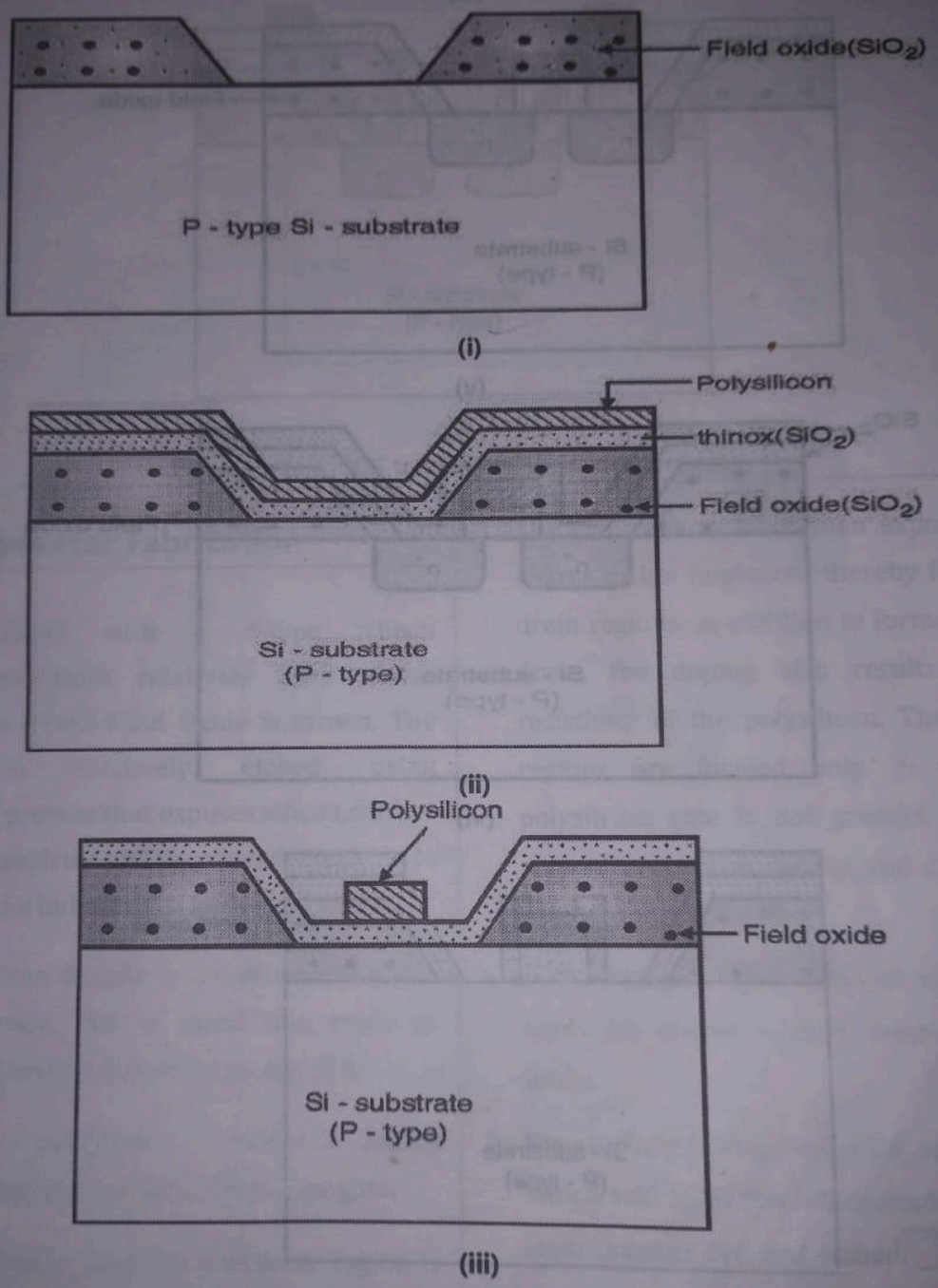
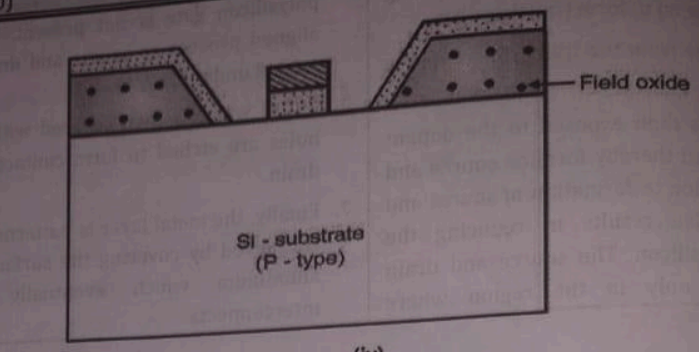


Fig. 2.21.1 Contd...



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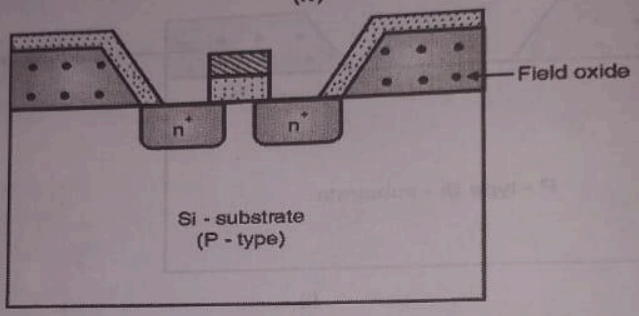

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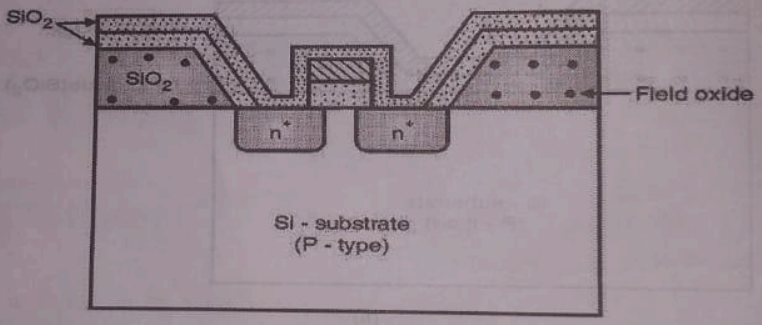

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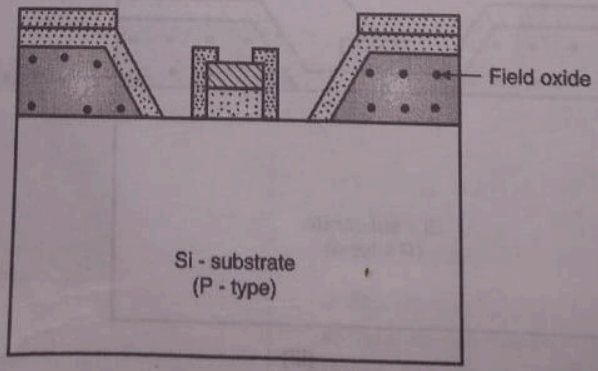

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Fig. 2.21.1 Contd...

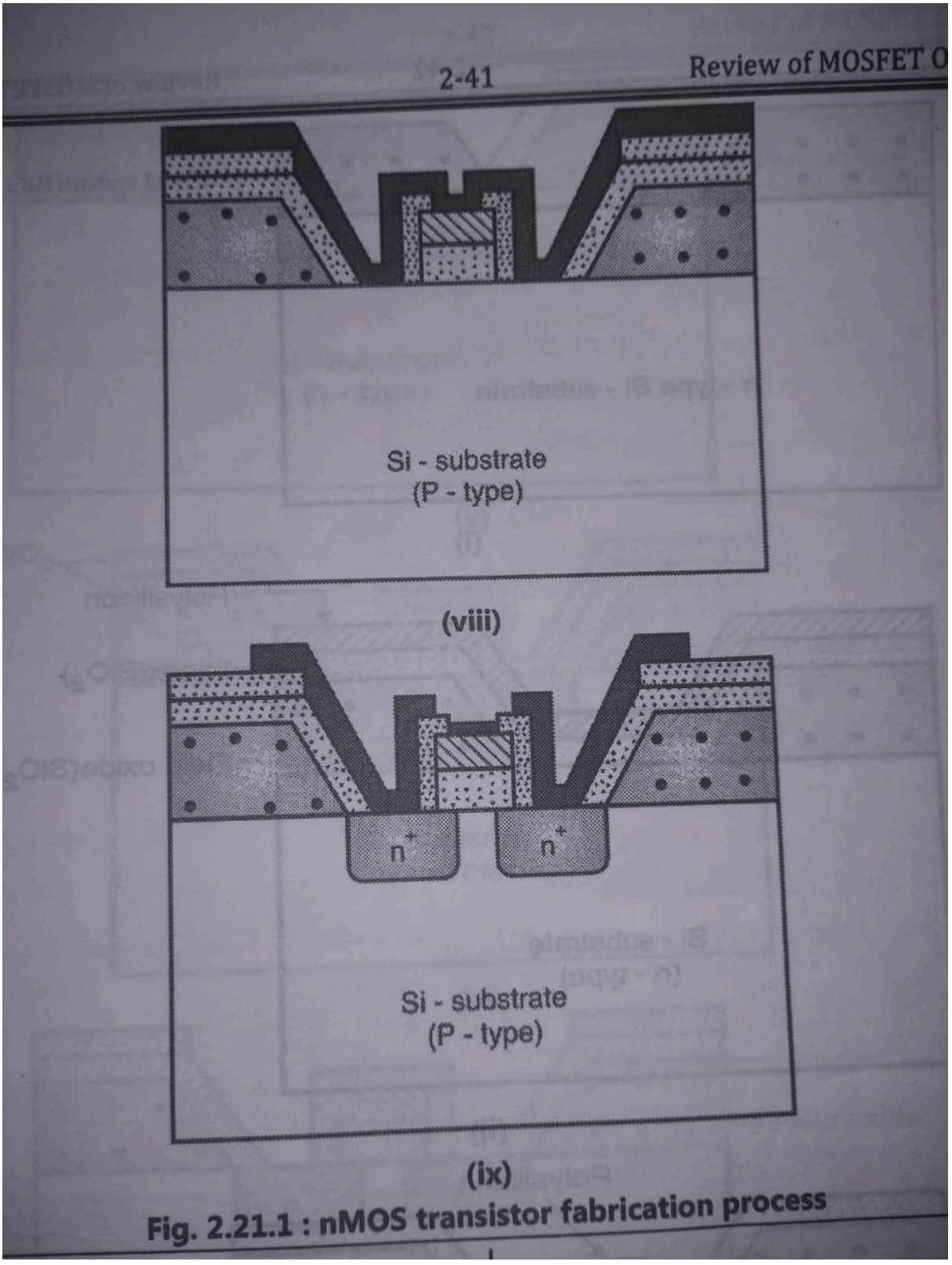

Fig. 2.21.1 : nMOS transistor fabrication process

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P-Well Fabrication Process: Easy Explanation

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The **p-well** fabrication process is used in CMOS (Complementary Metal-Oxide-Semiconductor) technology to create the n-type regions where NMOS transistors will be formed. Here's a simple, step-by-step explanation:

1. **Start with a N-Type Wafer:**
    - Begin with an **n-type silicon wafer**. This means the wafer is mostly made of n-type silicon.
2. **Grow a Thick Oxide Layer:**
    - Grow a **thick silicon dioxide (SiO_2) layer** on the wafer. This layer is called **field oxide** and is used to isolate different areas of the wafer.
3. **Pattern the Field Oxide:**
    - Use a **photolithography process** to pattern and etch away parts of the field oxide. This exposes the silicon where the p-well will be created.
4. **Create the P-Well:**
    - **Diffuse or implant p-type dopants** (such as boron) into the exposed silicon areas. This creates the **p-well** regions. The p-well is an area of p-type silicon where PMOS transistors will be formed.
5. **Grow a Thin Oxide Layer:**
    - Grow a thin layer of silicon dioxide (called **thin oxide**) over the entire wafer, including the p-well regions. This thin oxide will later help in forming the transistor gates.
6. **Deposit Polysilicon:**
    - Deposit a layer of **polysilicon** on top of the thin oxide. This polysilicon layer will be used to form the gates of the transistors.
7. **Pattern Polysilicon:**
    - Use photolithography to pattern and etch the polysilicon layer to form the gates for the PMOS transistors.
8. **Form Source and Drain Regions:**
    - After forming the gates, **implant n-type dopants** in the regions where the source and drain of the NMOS transistors will be. This ensures that these regions are properly doped.
9. **Add Contacts and Metal Layers:**
    - Cover the wafer with an additional **SiO_2 layer** and etch contact holes. Deposit a **metal layer** (usually aluminum) and pattern it to form the electrical connections (interconnects).

The cross section of the finished n-well process is shown in Fig. 2.26.1. In a p-well process, the n-type substrate is normally connected to the positive supply (V_{DD}). On the other hand, the well has to be connected to the negative supply (V_{SS}). The V_{SS} and V_{DD} contacts are shown in the Fig. 2.26.1.

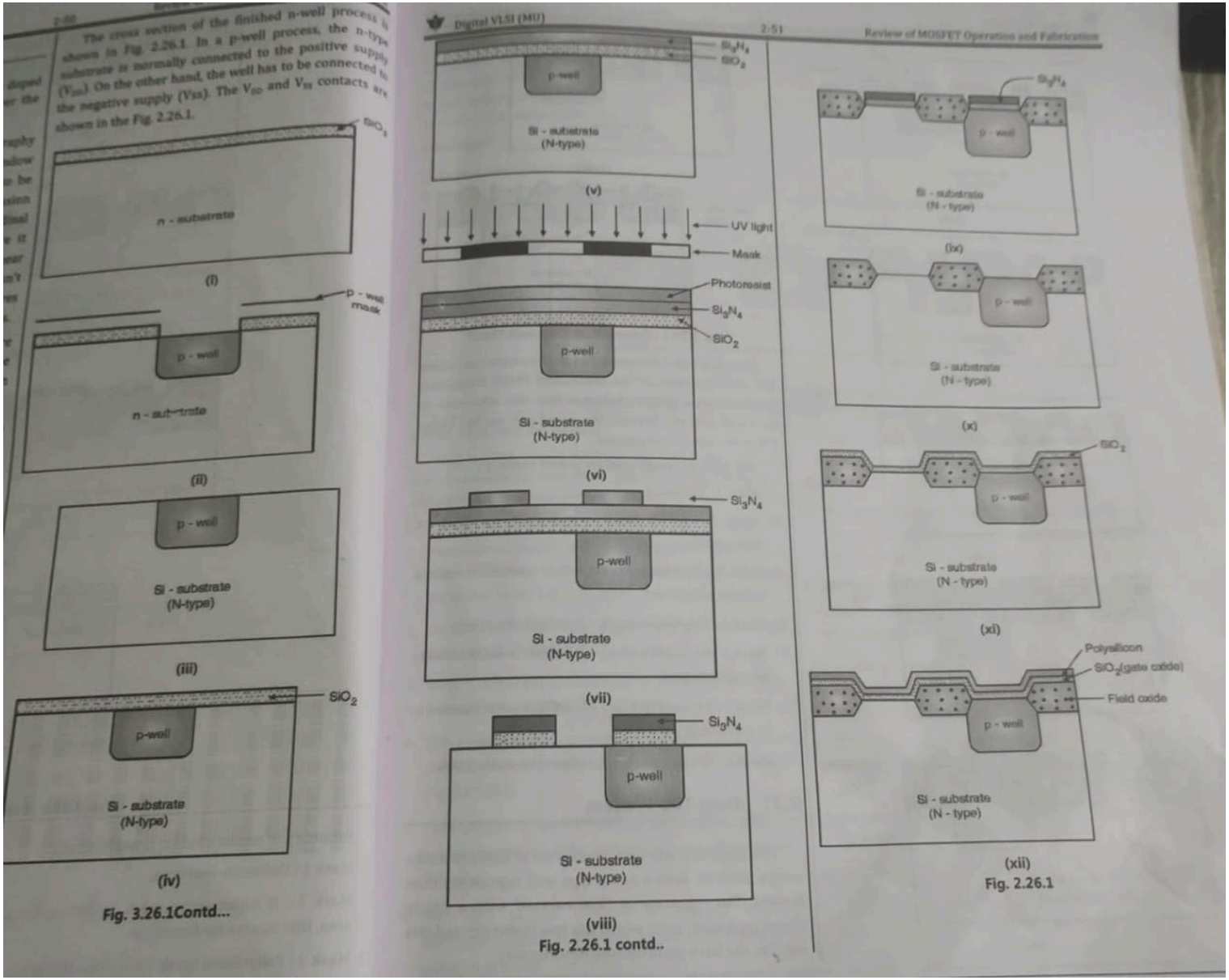

Fig. 3.26.1Contd...

Fig. 2.26.1 contd..

Fig. 2.26.1

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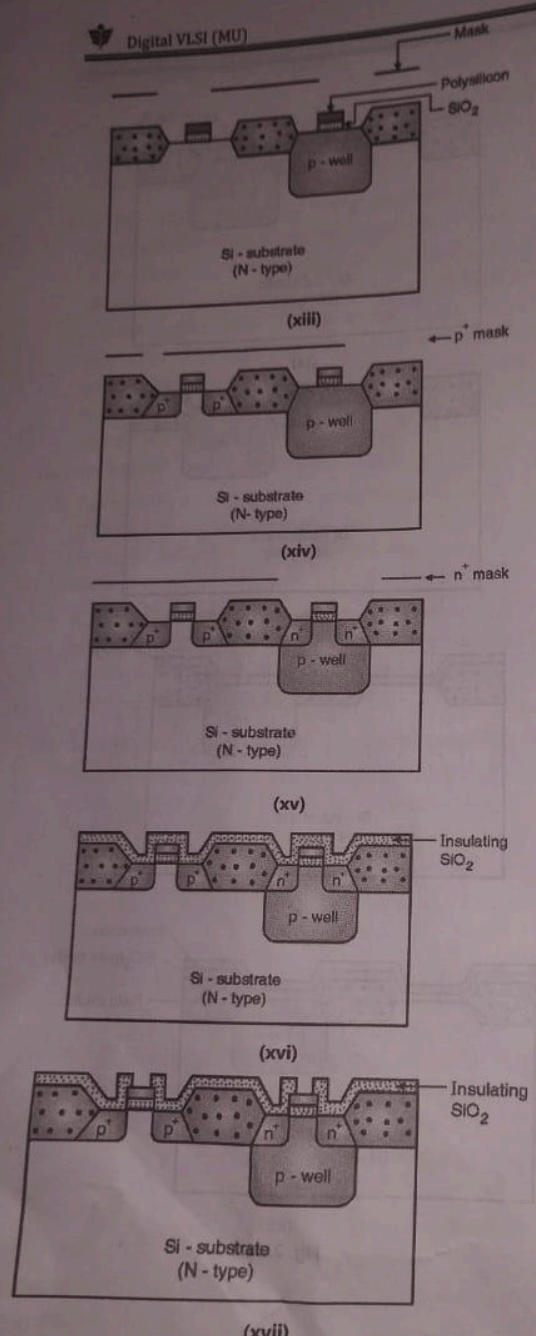

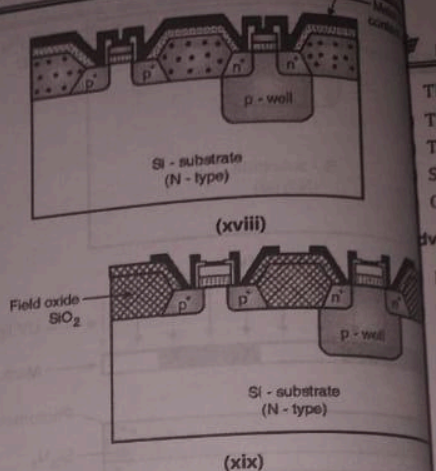

Fig. 2.26.1 : Process flow for p-well CMOS

p-well process are preferred in circumstances the characteristics of the NMOS and PMOS tran are required to be more balanced than that achiev an n-well process, because the p-well process has PMOS than an n-well process.

Summary of masks used for p-well process :

1) Mask 1 : Defines p-well area.
2) Mask 2 : Active mask – It defines the are transistors.
3) Mask 3 : Photoresist mask – It is used for thre voltage adjusment.
4) Mask 4 : Polysilicon mask – It defines the gates.
5) Mask 5 : n+ mask(n-plus) – It defines areas that be implanted n+.
6) Mask 6 : p+ mask(p-plus) – It defines areas that be implanted p+.
7) Mask 7 : Contact mask – It defines the contact cut

2.27 Twin Tub Process

This process starts with a substrate of high resis n-type material. Both n and p type well regions are created. The substrate is then covered with a li doped (epitaxial) layer which has low resistivity and reduces the latch-up problems considerably.

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Module 2

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1) B Draw and explain CMOS inverter with transfer characteristic. Find the condition For symmetric inverter.10

2)Draw and explain VTC characteristics of CMOS inverter in detail.

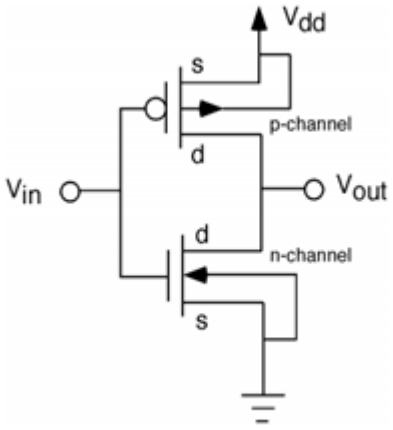


Fig7. Circuit diagram of CMOS Inverter

CMOS Inverter:

A CMOS inverter is a fundamental building block in digital logic circuits, composed of two transistors: a PMOS (p-channel MOSFET) and an NMOS (n-channel MOSFET). The inverter operates in such a way that when the input is high, the output is low, and when the input is low, the output is high, essentially "inverting" the input signal.

Circuit Structure:

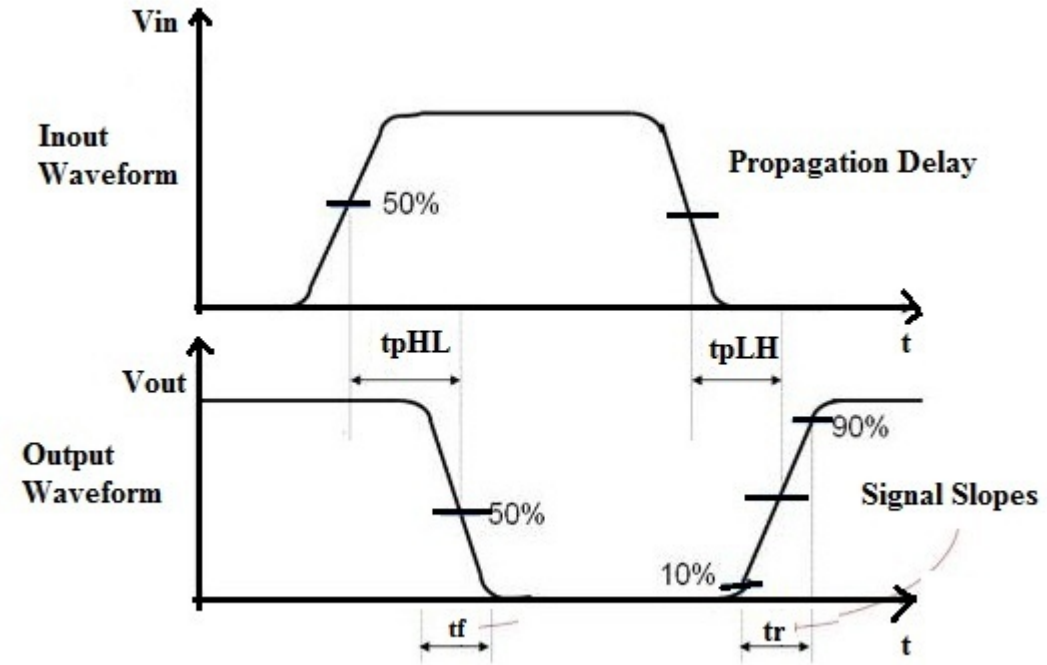
1. **PMOS Transistor**: The source of the PMOS is connected to the supply voltage (VDD), and the drain is connected to the output.
2. **NMOS Transistor**: The drain of the NMOS is connected to the output, and the source is connected to ground (GND).
3. **Input**: The gate terminals of both transistors are connected to the input signal (Vin).
4. **Output**: The output is taken from the connection point of the drain terminals of the PMOS and NMOS transistors.

Working of CMOS Inverter:

- **When Vin is low (0)**: The PMOS transistor turns ON (since it is turned on with low gate voltage), and the NMOS turns OFF (since it needs a high voltage at the gate to turn on). The output (Vout) is connected to VDD through the PMOS, resulting in a high output (logic 1).
- **When Vin is high (VDD)**: The NMOS transistor turns ON, and the PMOS transistor turns OFF. The output is connected to ground (GND) through the NMOS, resulting in a low output (logic 0).

Transfer Characteristic:

The transfer characteristic of a CMOS inverter is a graph of the output voltage (Vout) as a function of the input voltage (Vin). It shows the following regions:



1. **Region 1 (PMOS ON, NMOS OFF)**: When Vin is low (0 to a certain threshold), the PMOS is conducting and pulls the output high (Vout = VDD), while the NMOS is off.
2. **Region 2 (Transition region)**: As Vin increases, both transistors partially conduct. This creates a gradual transition in Vout as the input voltage rises. This region is where the inverter switches its state.
3. **Region 3 (PMOS OFF, NMOS ON)**: When Vin reaches a high voltage (near VDD), the NMOS transistor is fully ON, pulling the output low (Vout = 0), and the PMOS is off.

Condition for Symmetric Inverter:

For a symmetric CMOS inverter, the switching threshold (Vth) should be at half the supply voltage (VDD/2). This condition is achieved when:

1. **(W/L)p = (W/L)n**: The ratio of the width (W) to length (L) of the PMOS and NMOS transistors must be adjusted such that the drive strength of both transistors is equal. This ensures that the inverter switches symmetrically around VDD/2.
2. **μn/μp = (W/L)p / (W/L)n**: The mobility (μ) of electrons (in NMOS) and holes (in PMOS) differs, so to achieve symmetry, the width-to-length ratio of the PMOS must be larger than that of the NMOS. Typically, this ratio is adjusted to account for the lower hole mobility (μp) compared to electron mobility (μn).

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Q3)Compare the effect of Full scaling and Constant voltage scaling on Current, Power, power density. State which is more power efficient.

Parameters	Before Scaling	After scaling	
		Full scaling	Constant Voltage scaling
Channel length	L	$L' = L/s$	$L' = L/s$
Channel width	W	$W' = W/s$	$W' = W/s$
Gate oxide thickness	tox	$tox' = tox/s$	$tox' = tox/s$
Junction depth	Xj	$Xj' = Xj/s$	$Xj' = Xj/s$
Power supply voltage	VDD	$VDD' = VDD/s$	$VDD' = VDD$
Threshold voltage	VT0	$VT0' = VT0/s$	$VT0' = VT0$
Doping densities	N_A, N_D	$N_A', N_D' = sN_A , sN_D$	$N_A', N_D' = s^2 N_A , s^2 N_D$
Oxide capacitance	Cox	$Cox' = Cox/s$	$Cox' = Cox/s$
Drain current	I_D	$I_D' = I_D/s$	$I_D' = s.I_D$
Power dissipation	P_D	$P_D' = P_D/s^2$	$P_D' = s. P_D$
Power density	P_D/Area	P_D/Area' = P_D/Area	P_D/Area' = s^3. P_D/Area

Effects of Scaling in MOSFETs :

Scaling in MOSFETs means reducing the size of the transistors to make circuits smaller, faster, and more efficient. There are two main types of scaling: **Full Scaling** and **Constant Voltage Scaling**.

1. Full Scaling:

- In **full scaling**, everything—transistor size, supply voltage (VDD), and threshold voltage (Vth)—is reduced by the same factor (let's call it 's').
- **Key Points**:

    - **Area**: The area of the MOSFET becomes smaller by 1s2\frac{1}{s^2}s21, which means more transistors can fit on a chip.
    - **Current Density**: Current density (how much current flows through a given area) increases by sss, but this is manageable since both voltage and current reduce evenly.
- **Benefits**:
    - **Lower Power**: Power consumption goes down because both voltage and size are scaled down.
    - **No Reliability Issues**: The electric fields inside the transistor stay the same, so there are fewer problems like heat damage or breakdowns.

2. Constant Voltage Scaling:

- In **constant voltage scaling**, only the size of the transistor is reduced, but the supply voltage (VDD) stays the same.
- **Key Points**:
    - **Area**: Like full scaling, the area reduces by 1s2\frac{1}{s^2}s21, so more transistors fit on the chip.
    - **Current Density**: Current density increases by s3s^3s3, meaning more current flows through the smaller area, which increases the stress on the transistor.
- **Drawbacks**:
    - **Higher Power Density**: Power density (power per unit area) increases significantly, which can lead to **reliability problems** such as:
        - **Electromigration** (damage to wires due to high current),
        - **Hot Carrier Effects** (damage from high-energy electrons),
        - **Oxide Breakdown** (failure of the insulating layer),
        - **Electrical Overstress** (too much voltage or current causing damage).

In short, **full scaling** reduces power and keeps the device safe, while **constant voltage scaling** increases the risk of damage due to higher power density.

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Module 3

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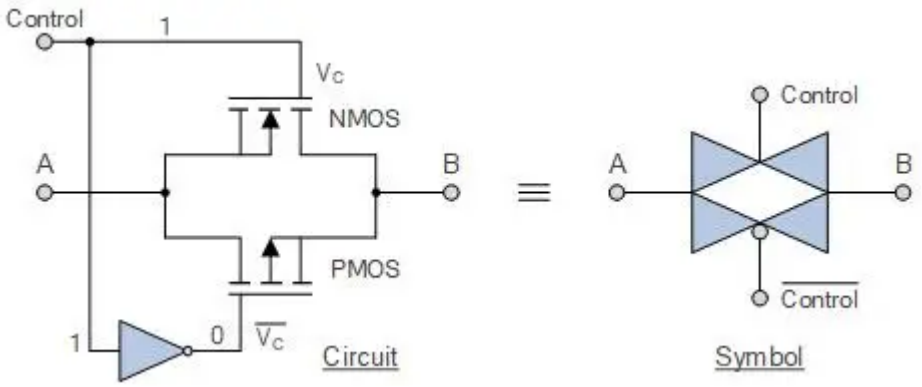
1) State Working of TG logic with proper diagram **(5)**



Working of Transmission Gate (TG) Logic:

A **Transmission Gate** (TG) consists of two transistors: an **NMOS** and a **PMOS**, connected in parallel. The key point of a transmission gate is that it allows signals to pass when it is "enabled" and blocks them when "disabled."

1. **NMOS and PMOS in Parallel**:
    - The NMOS transistor passes a strong '0' (low signal) but weakly passes a '1' (high signal).
    - The PMOS transistor, on the other hand, passes a strong '1' but weakly passes a '0'.
    - When both are combined, they effectively pass both logic '1' and '0' signals equally well, ensuring that there's minimal signal degradation.
2. **Control Signals**:
    - The **control signal** (Vc) determines whether the gate is ON or OFF. If the control signal is high (Vc = 1), both NMOS and PMOS are turned ON, allowing the signal at input A to pass through to output B.
    - When the control signal is low (Vc = 0), both transistors are OFF, and the signal does not pass through.

Summary of Operation:

- **Control = 1**: The transmission gate conducts, and the signal from A is transferred to B (A = B).
- **Control = 0**: The transmission gate is off, and no signal is transferred from A to B (A is disconnected from B).

Advantages:

- Transmission gates are widely used in multiplexers, flip-flops, and pass-gate logic due to their ability to pass both logic levels without distortion.

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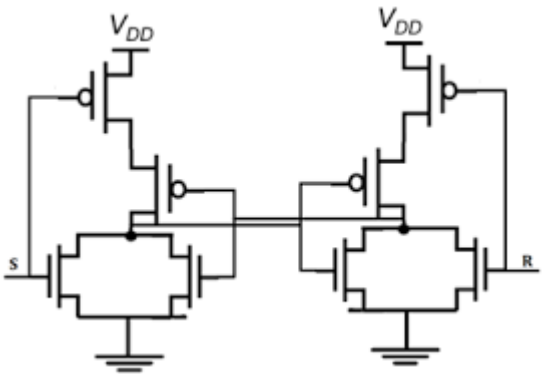
2) Design SR Latch using CMOS logic and draw its layout 10]

7)Realize s r flip flop using cmos logic And draw it's layout. 10



SR Latch Using CMOS Logic:

The **SR Latch** is a basic type of flip-flop that stores a single bit of data. It has two inputs, **S (Set)** and **R (Reset)**, and two outputs, **Q** and **Q'** (the complement of Q).

CMOS Design:

- The **CMOS SR latch** uses **CMOS NOR gates**. Each NOR gate is designed using a combination of **PMOS** and **NMOS transistors**.
- In the diagram:
    - **PMOS transistors** are typically at the top, connected to **VDD** (the supply voltage).
    - **NMOS transistors** are at the bottom, connected to **ground**.

In this SR latch:

- **S** is the input to the first NOR gate, and **R** is the input to the second NOR gate.
- The output **Q** of the first NOR gate is connected to the input of the second NOR gate, and the output **Q'** of the second NOR gate is connected to the input of the first NOR gate, creating feedback between the gates.

Working of SR Latch:

1. **S = 1, R = 0**: The latch is set. **Q = 1**, and **Q' = 0**.
2. **S = 0, R = 1**: The latch is reset. **Q = 0**, and **Q' = 1**.
3. **S = 0, R = 0**: The latch maintains its current state.

4. **S = 1, R = 1**: This is an invalid condition for the basic SR latch (both outputs will be 0), which should be avoided.

Layout Design:

- To design the **layout** of this SR latch in CMOS, you'd arrange the PMOS and NMOS transistors in such a way that the NOR gates are implemented using the **pull-up (PMOS)** and **pull-down (NMOS)** network.
- The layout would include:
    - **Metal layers** for connections,
    - **Active regions** for the PMOS and NMOS transistors,
    - **Poly gates** for forming the transistor gates.

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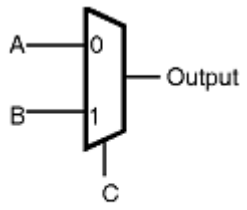
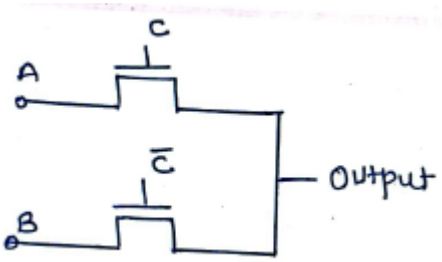
3) Implement using CMOS logic 1) 1-Bit full adder 2) DFF using TG. [10]

==========

4) Realize 2:1 mux using TG. 5



2 : 1 MUX



Working Principle of a 2:1 MUX Using Transmission Gates:

1. **Multiplexer Functionality**:
    - A 2:1 MUX has two data inputs (A and B), one control signal (C), and one output (Y).
    - The control signal (C) determines which input (A or B) is connected to the output.
        - When control signal C = 0 (low), the MUX selects input A.
        - When control signal C = 1 (high), the MUX selects input B.
2. **Using Transmission Gates**:
    - Transmission gates are made using complementary MOSFETs (nMOS and pMOS) connected in parallel.

    - Transmission gates allow a signal to pass through without significant loss, unlike single MOSFETs, which have threshold voltage drops.
    - In the 2:1 MUX using transmission gates:
        - One transmission gate is connected between input A and the output, controlled by the control signal C.
        - The other transmission gate is connected between input B and the output, controlled by the inverted control signal C¯\overline{C}C.
3. **Operation**:
    - When C = 1 (high):
        - The transmission gate connected to input B is turned on, allowing B to pass to the output.
        - The transmission gate connected to input A is turned off, blocking A.
    - When C = 0 (low):
        - The transmission gate connected to input A is turned on, allowing A to pass to the output.
        - The transmission gate connected to input B is turned off, blocking B.

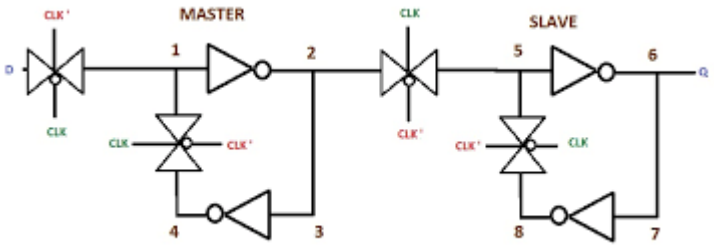
Advantages of Using Transmission Gates:

- **Low power dissipation**: Transmission gates consume less power compared to using traditional logic gates.
- **Rail-to-rail swing**: The signal can pass through without attenuation of the voltage levels, maintaining full rail-to-rail swing.
- **Efficient design**: The transmission gate MUX requires fewer components, which can reduce the overall area and complexity of the circuit.
- **Bidirectional signal flow**: Transmission gates allow for bidirectional signal flow, which can be beneficial in certain applications.

By implementing this approach using TGs, the MUX provides an efficient way to select between two inputs, with a simple and power-efficient circuit design.

==========

5) Realize the following 2) DFF using TG [10]



Realization of D Flip-Flop (DFF) Using Transmission Gates (TG):Working Principle:

- A **D flip-flop (DFF)** stores and transfers data on the rising or falling edge of a clock signal. It consists of two stages: a master and a slave latch.
- The **master stage** captures the input data (D) when the clock (CLK) is low, while the **slave stage** transfers the data to the output (Q) when the clock is high.

Using Transmission Gates:

- Transmission gates are used to control the flow of data through the flip-flop based on the clock signal.
- In the **master stage**, the TGs allow data (D) to be latched when CLK is low.
- In the **slave stage**, the TGs allow the stored data to be passed to the output (Q) when CLK is high.

Operation:

1. When **CLK is low**:
    - The transmission gate connected to the master stage (1-2) is ON, allowing the input D to be stored at the intermediate point (2).
    - The slave stage remains off, preventing the output from updating.
2. When **CLK transitions to high**:
    - The master stage becomes OFF, latching the data.
    - The slave stage is ON, allowing the latched data to be transferred to the output (Q).

Explanation of the Diagram:

- The diagram shows two transmission gates in the master and slave stages.
    - **Master**: The first pair of TGs (1-2 and 3-4) control the data flow into the master latch.
    - **Slave**: The second pair of TGs (5-6 and 7-8) control the data flow to the output.
- The clock signals **CLK** and **CLK'** (inverted clock) control when the data is latched and when it is passed to the output.

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This is a correct implementation of a D flip-flop using transmission gates. For your exam, you can describe the operation as outlined above, and mention how the transmission gates control the flow of data through the master and slave stages.

Advantages of TG-Based DFF:

- Transmission gates provide low-power operation.
- They offer efficient rail-to-rail switching with minimal voltage loss.

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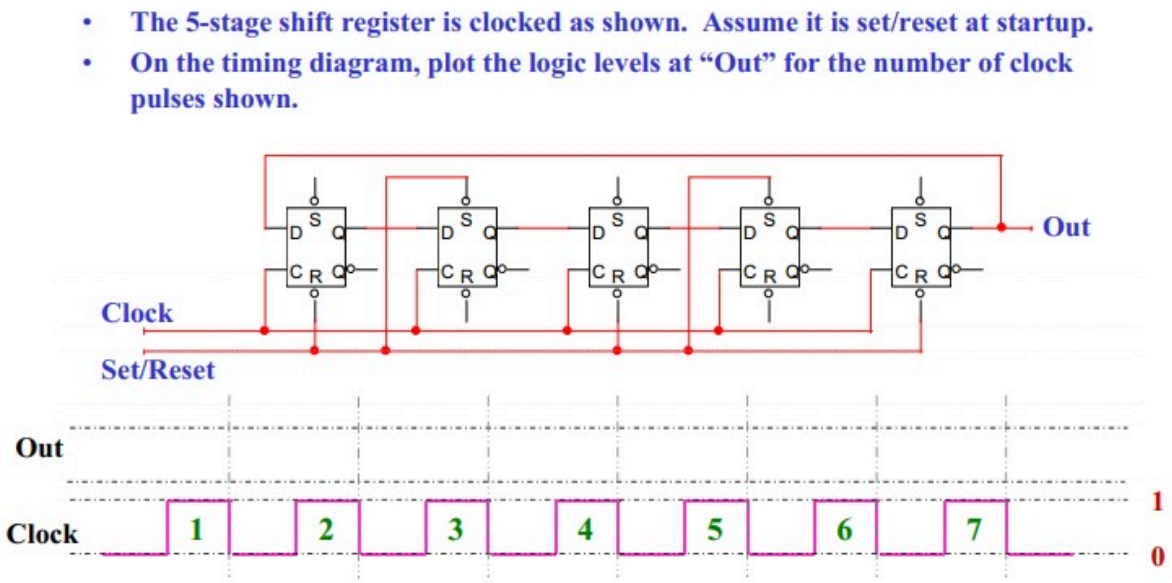
6) 1 bit 5 stage shift register.



A **shift register** is a sequential logic circuit that shifts the input data bit through a series of flip-flops on each clock cycle. A 1-bit 5-stage shift register consists of **five D flip-flops (DFFs)** connected in series.

Working Principle:

- **Input (D)**: The input bit is provided to the first D flip-flop (DFF1).
- **Shifting**: On every clock pulse, the bit stored in each flip-flop is shifted to the next flip-flop.
- **Stages**: After each clock cycle, the input bit moves one stage forward.
- **Output (Q)**: After five clock pulses, the bit from the input appears at the output of the fifth flip-flop (DFF5).

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Operation:

1. **Clock Cycle 1**: The input bit is loaded into DFF1.
2. **Clock Cycle 2**: The bit shifts from DFF1 to DFF2.
3. **Clock Cycle 3**: The bit shifts from DFF2 to DFF3.
4. **Clock Cycle 4**: The bit shifts from DFF3 to DFF4.
5. **Clock Cycle 5**: The bit shifts from DFF4 to DFF5 and appears at the output.

Each flip-flop holds the bit for one clock cycle before passing it to the next stage.

Applications:

- **Data Storage**: Temporary storage and delay of data.
- **Data Transfer**: Serial-to-parallel or parallel-to-serial data conversion.
- **Digital Systems**: Used in communication systems and digital signal processing.

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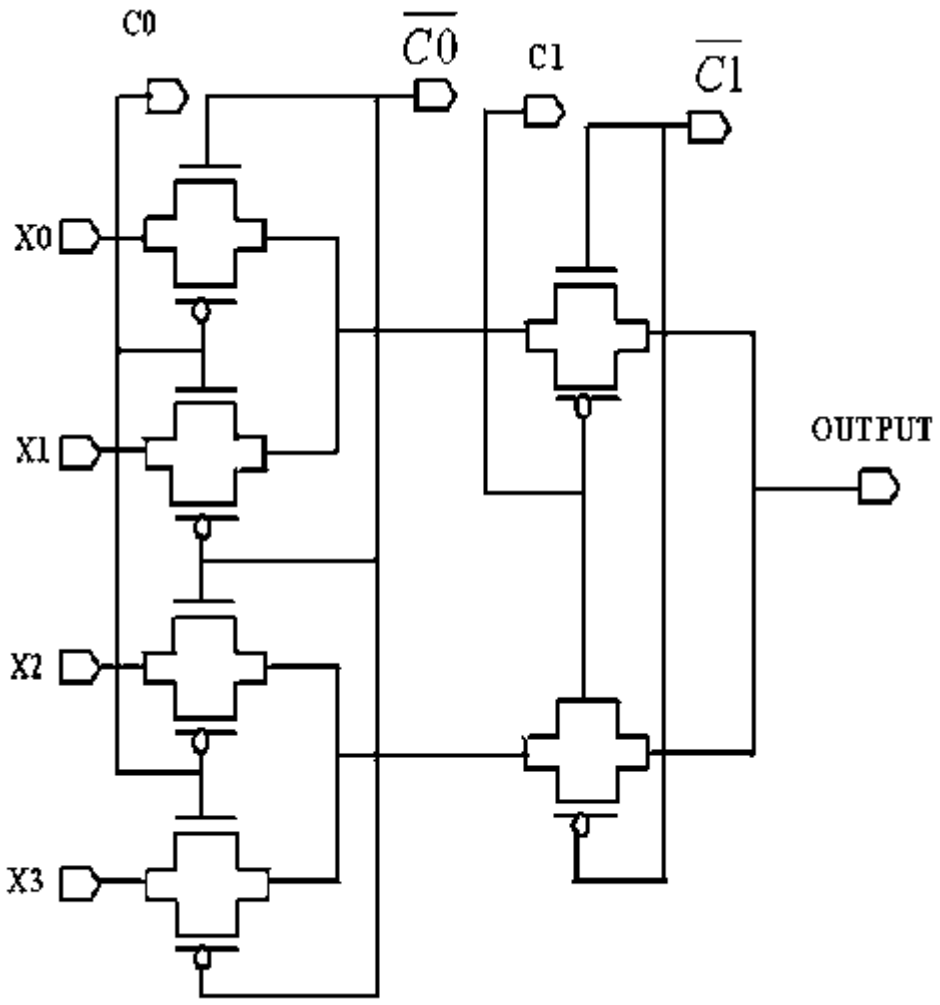
8)mplement 4:1 mux using TG.



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Components:

- A 4:1 MUX has 4 data inputs (D0, D1, D2, D3), 2 select lines (S1, S0), and 1 output (Y).
- Transmission gates (TG) are used to pass or block signals based on control inputs.

4:1 MUX using Transmission Gates:

1. **Select Lines (S1, S0):**
    - The select lines S1 and S0 determine which data input (D0, D1, D2, D3) gets connected to the output.
2. **Transmission Gate Logic:**
    - A transmission gate consists of a PMOS and NMOS transistor in parallel.
    - The NMOS is activated by the control signal (S), while the PMOS is activated by the complement of the control signal (S¯\overline{S}S).
3. **Circuit Description:**
    - For each data input (D0, D1, D2, D3), use one transmission gate. The control logic for each transmission gate is derived from the select lines (S1 and S0).
    - The inputs are controlled as follows:
        - D0 is selected when S1¯\overline{S1}S1 and S0¯\overline{S0}S0 are high.
        - D1 is selected when S1¯\overline{S1}S1 and S0 are high.
        - D2 is selected when S1 and S0¯\overline{S0}S0 are high.
        - D3 is selected when S1 and S0 are high.
4. **Truth Table:**

S1	S0	Selected Input
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Transmission Gate Implementation:

- For **D0**: Connect D0 to the output using a TG controlled by S1¯\overline{S1}S1 and S0¯\overline{S0}S0.
- For **D1**: Connect D1 to the output using a TG controlled by S1¯\overline{S1}S1 and S0.

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    - For **D2**: Connect D2 to the output using a TG controlled by S1 and S0¯\overline{S0}S0.
    - For **D3**: Connect D3 to the output using a TG controlled by S1 and S0.

Diagram:

- You can draw the 4 TGs connected in parallel, each controlled by the appropriate combination of select lines and their complements, with the output being driven by the selected input.

Summary for Exam Answer:

- **4:1 MUX using Transmission Gates**: Four transmission gates are used, one for each data input (D0, D1, D2, D3). The gates are controlled by the select lines (S1, S0) and their complements. Based on the select lines, one of the data inputs is passed to the output through the transmission gate, realizing a 4:1 multiplexer.

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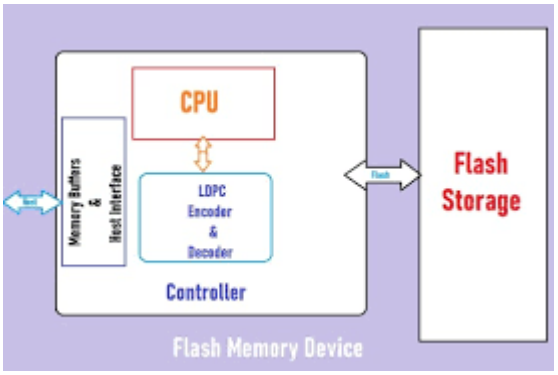
Module 4

==========

1) Explain Flash memory in brief.



Flash memory is a type of **non-volatile memory** that retains data even after the power is turned off. It is commonly used in USB drives, SSDs, memory cards, and embedded systems. Flash memory is based on **floating-gate transistors** that can hold an electrical charge, representing binary data (0s and 1s).

Key Points for Exam:

1. **Non-volatile**: Retains data without power.
2. **Types**:
    - **NAND flash**: Used in SSDs, memory cards. Offers higher storage density.
    - **NOR flash**: Used in devices requiring faster read speeds, such as firmware storage.
3. **Write/Erase Cycles**: Flash memory can be written to and erased in blocks, with a limited number of write cycles (endurance).
4. **Applications**: Used in smartphones, computers, cameras, and embedded systems for data storage.

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2) Draw and explain 6-T SRAM with neat and clean diagram. Explain read and Write condition with equations.10

8) Explain 6T sram with its read and write ooperation.10

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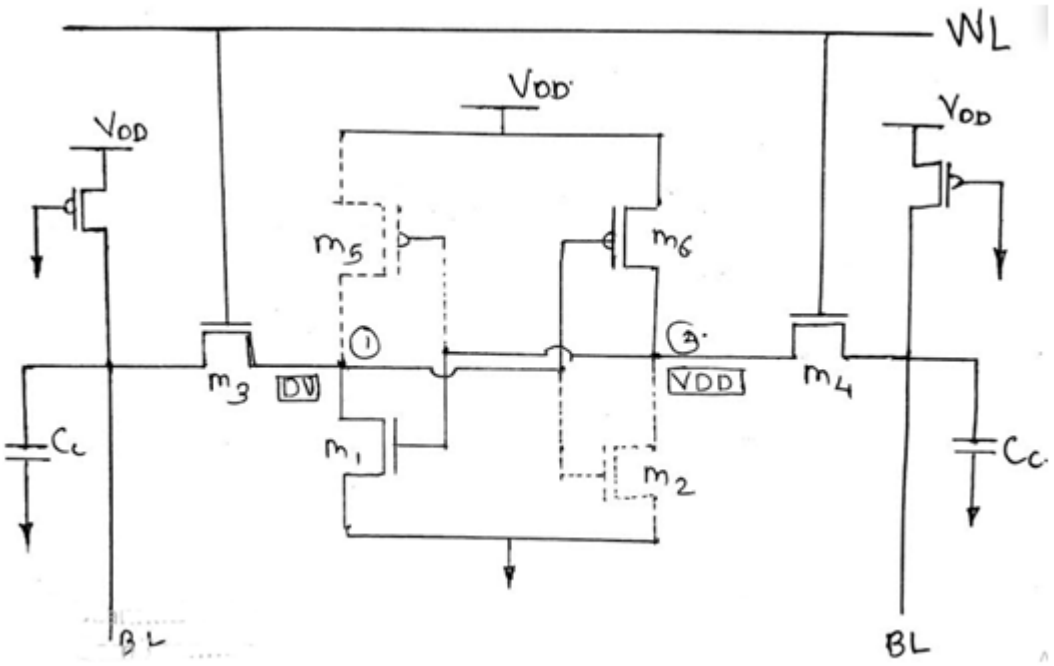

6-T SRAM (Static Random Access Memory) Explanation:

A **6-T SRAM cell** consists of **six transistors**, where four transistors form two cross-coupled inverters and the remaining two transistors are used for access control during read and write operations.

Structure of 6-T SRAM:

- **Cross-coupled Inverters**: Two nMOS and two pMOS transistors form a pair of inverters connected in a feedback loop. This structure ensures that the cell retains its state (either 0 or 1) as long as power is supplied.
- **Access Transistors**: The other two nMOS transistors (controlled by the word line, WL) are used to control access to the storage nodes during read and write operations.

Working of SRAM:

1. **Write Operation**:
    - **Condition**: To write data into the SRAM cell, the word line (WL) is enabled (set high), allowing access to the bit lines (BL and BL¯\overline{BL}BL).
    - If the data to be written is a 1:
        - BL is driven high, and BL¯\overline{BL}BL is driven low.
        - The access transistors pass these signals to the cross-coupled inverters, forcing one inverter node to a high voltage (logic 1) and the other to a low voltage (logic 0).

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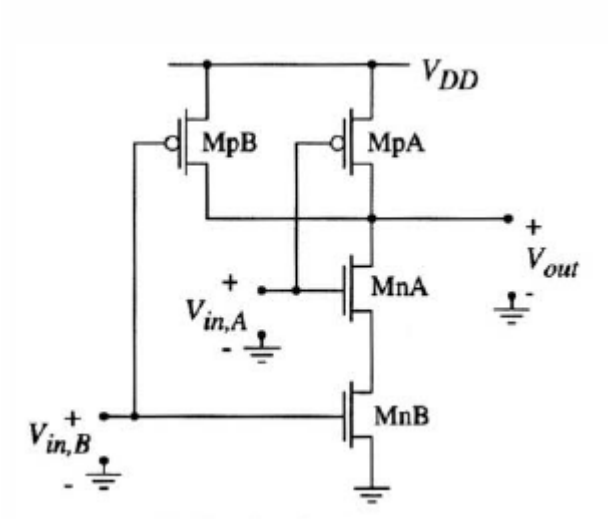
    - If the data to be written is a 0:
        - BL is driven low, and BL¯\overline{BL}BL is driven high, flipping the state of the cross-coupled inverters.
2. **Equation for Write Condition**:
    - When WL = 1, data is written to the cell, and the value stored is determined by the state of BL and BL¯\overline{BL}BL.
3. **Read Operation**:
    - **Condition**: During a read operation, the word line (WL) is again set high to enable the access transistors, and the bit lines (BL and BL¯\overline{BL}BL) are precharged to a known voltage (usually high).
    - The voltage at the storage nodes will then either pull BL down (if the stored bit is 0) or leave BL high (if the stored bit is 1).
    - A sense amplifier connected to BL and BL¯\overline{BL}BL detects the voltage difference to determine whether a 0 or 1 is stored in the cell.
4. **Equation for Read Condition**:
    - When WL = 1, if BL = 1, the stored bit is 1; if BL = 0, the stored bit is 0.

Summary:

- **6-T SRAM** uses six transistors: two for data storage (cross-coupled inverters) and two for read/write access (access transistors).
- **Write Operation**: Data is written by controlling the bit lines BL and BL¯\overline{BL}BL while WL is enabled.
- **Read Operation**: Data is read by sensing the voltage difference on BL and BL¯\overline{BL}BL after WL is enabled.

==========

3) Draw and Explain the working of NAND based Flash memory.5



$V_{in,A}$	$V_{in,B}$	V_{out}
0v	0v	V_{DD}
0v	V_{DD}	V_{DD}
V_{DD}	0v	V_{DD}
V_{DD}	V_{DD}	0v

NAND-Based Flash Memory

NAND flash memory is a type of non-volatile storage technology that retains data even when power is removed. It is widely used in USB drives, SSDs (Solid State Drives), and memory cards due to its high storage density and efficiency. Here's an explanation of its working:

1. Structure:

- **Memory Cells**: NAND flash memory consists of memory cells arranged in a series of pages, which are grouped into blocks. Each memory cell is based on floating-gate transistors that can hold an electrical charge.
- **Bitlines and Wordlines**: Cells are organized into rows (wordlines) and columns (bitlines) to facilitate access.

2. Programming (Writing Data):

- **Applying Voltage**: To write data to a NAND cell, a high voltage is applied to the control gate of the selected cell while the source terminal is grounded. This process injects electrons into the floating gate, changing the threshold voltage of the cell.
- **Storing Data**: The presence of charge in the floating gate represents a '0' or '1':
    - **Charged Floating Gate**: Represents a '0'.
    - **Uncharged Floating Gate**: Represents a '1'.

3. Reading Data:

- **Selecting the Cell**: To read data, a voltage is applied to the wordline of the selected cell while the bitline is monitored.

- **Current Flow**: If the floating gate is charged (indicating a stored '0'), the cell will not conduct current, and a low voltage will be detected on the bitline. If the floating gate is uncharged (indicating a stored '1'), the cell will conduct, resulting in a high voltage on the bitline.

4. Erasing Data:

- **Erasing Blocks**: NAND flash memory erases data in blocks, not individual cells. A high voltage is applied to the source of all cells in the block, allowing electrons to escape the floating gate.
- **Resetting Cells**: This process restores the floating gates to their uncharged state, effectively resetting all bits in the block to '1'.

5. Advantages of NAND Flash:

- **High Density**: NAND flash can store a large amount of data in a small physical space, making it suitable for portable devices.
- **Low Cost**: The compact design and mass production have led to lower costs compared to other storage technologies.
- **Performance**: NAND flash offers faster write and read speeds compared to traditional hard drives.

Summary for Exam:

- **NAND Flash Memory**: A non-volatile storage technology consisting of floating-gate transistors arranged in a grid format.
- **Programming**: Involves injecting electrons into the floating gate to store data.
- **Reading**: Voltage applied to wordlines allows for current flow detection, indicating stored values.
- **Erasing**: Conducted in blocks, restoring cells to their original state.

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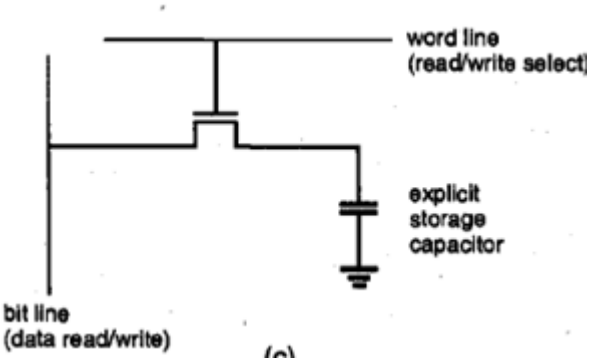
4) Explain 1T DRAM with its read and write operation, also draw the

layout. [10]



1T DRAM (Dynamic Random Access Memory)

Structure: A 1T DRAM cell consists of one transistor (M1) and one capacitor (C1). The capacitor stores the charge representing a data bit, while the transistor controls access to the cell.

Read Operation:

1. **Activate the Word Line (WL)**: A high voltage is applied to the word line, turning on the transistor (M1).
2. **Charge Detection**:
    - If the capacitor (C1) is charged (representing a '1'), it discharges through the bit line (BL), causing a voltage change detected by the sense amplifier.
    - If the capacitor is uncharged (representing a '0'), no significant voltage change occurs.
3. **Refresh Requirement**: Since charge leaks over time, the data must be refreshed periodically to maintain accuracy.

Write Operation:

1. **Activate the Word Line (WL)**: Apply a high voltage to turn on the transistor (M1).
2. **Data Input via Bit Line (BL)**:
    - To write a '1': Apply a high voltage to the bit line to charge the capacitor (C1).
    - To write a '0': Ground the bit line, discharging the capacitor.
3. **Deactivate the Word Line (WL)**: After writing, the word line is turned off, isolating the capacitor and preserving the stored charge.

Advantages:

- **High Density**: Compact cell structure allows for high storage capacity.
- **Simple Structure**: Fewer components simplify manufacturing.

Disadvantages:

- **Volatility**: Requires periodic refreshing due to charge leakage.
- **Slower Access Times**: Compared to SRAM, due to refresh cycles.

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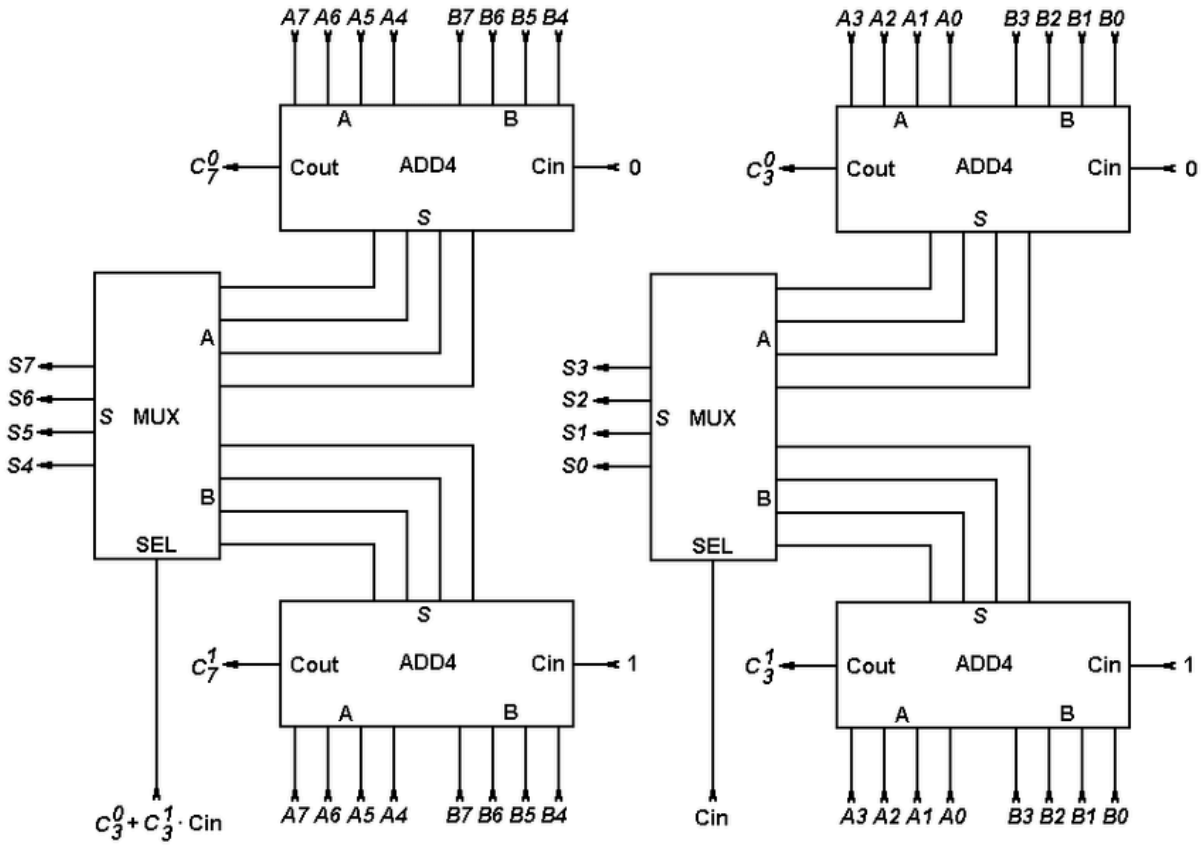
5) Implement 1) 8-bit carry select adder 2) 4-bit array multiplier [10]

1) 8-bit carry select adder



<u>4-bit array multiplier</u>

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7) Explain the working of floating gate Is transistor in flash memory.5

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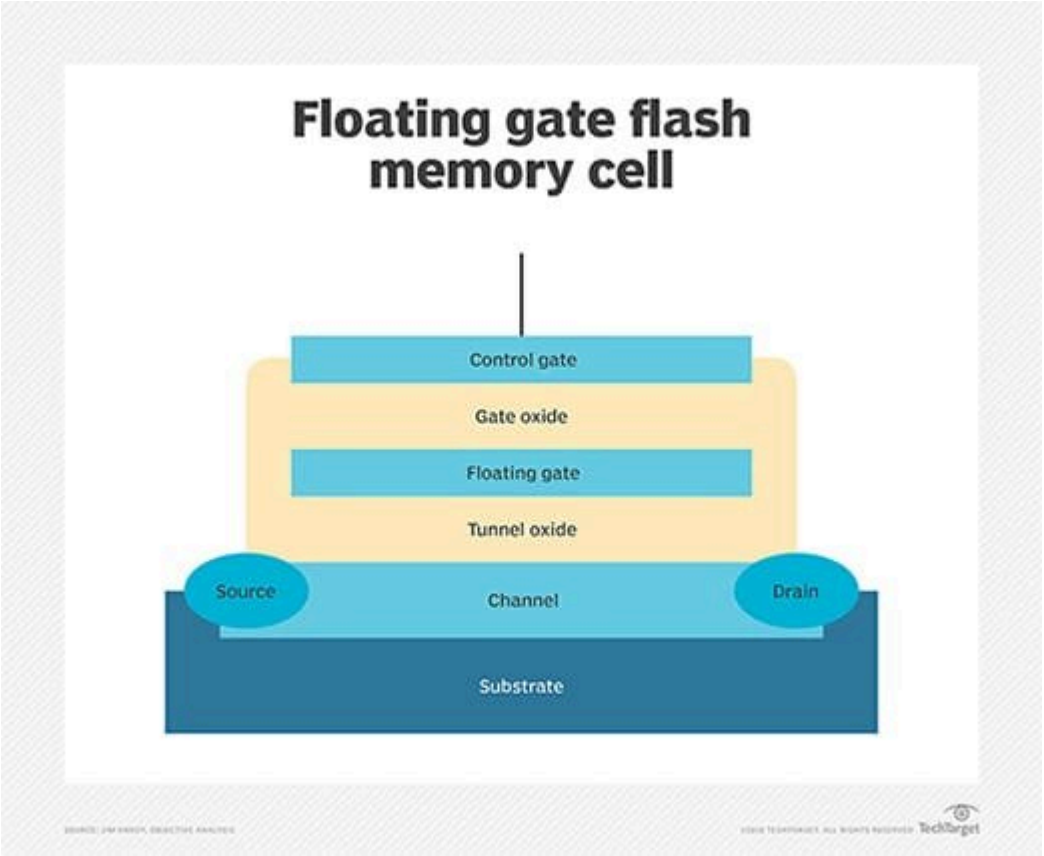

Floating Gate Transistor in Flash Memory

Structure:

- A floating gate transistor consists of a **control gate** (connected to the word line), a **floating gate** (isolated by insulating material), and a **channel** (for current flow).

Working Principle:

1. **Programming (Writing Data)**:
    - A high voltage is applied to the control gate, allowing electrons to tunnel into the floating gate.
    - **Charged Floating Gate**: Represents a '0'.
    - **Uncharged Floating Gate**: Represents a '1'.
2. **Reading Data**:
    - A lower voltage is applied to the control gate.
    - If the floating gate is charged (indicating a '0'), the transistor does not conduct, resulting in a low voltage on the bit line.
    - If the floating gate is uncharged (indicating a '1'), the transistor conducts, leading to a high voltage on the bit line.
3. **Erasing Data**:

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    - A high voltage is applied to the source, allowing electrons to escape from the floating gate, resetting it to an uncharged state (representing a '1').

Advantages:

- **Non-Volatility**: Retains data without power.
- **High Density**: Allows for compact memory cell design.

Summary for Exam:

- **Floating Gate Transistor**: Key component in flash memory for storing data.
- **Processes**: Programming (injects charge), Reading (detects charge state), Erasing (removes charge).

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Module 5

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1) Write short note on clock distribution.5

4) Explain clock distribution in vlsi design.5

Clock Distribution

Clock distribution is vital in digital circuits, ensuring that all components receive a synchronized clock signal to operate correctly.

Key Points:

1. **Purpose**:
    - Synchronizes various parts of a digital system, such as microprocessors and ASICs, by providing a common clock signal.
2. **Challenges**:
    - **Skew**: The difference in arrival time of the clock signal at different circuit parts can lead to timing errors.
    - **Jitter**: Variability in the clock signal due to noise can affect performance and reliability.
3. **Distribution Methods**:
    - **Hierarchical Distribution**: Employs multiple levels of clock trees to manage signal integrity and reduce load.
    - **Clock Buffers**: Amplify the clock signal to drive it over longer distances without degradation.
4. **Design Techniques**:
    - **H-tree and X-tree Structures**: Common topologies that help minimize skew by ensuring equal signal paths.
    - **Balanced Trees**: Designed to provide uniform propagation delay across the circuit.

Conclusion:

Effective clock distribution is crucial for high-speed operation and power efficiency in integrated circuits, directly impacting the performance and reliability of digital systems.

This note provides a clear overview of clock distribution for a 5-mark exam question.

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2) Ii) Implement carry circuit of 4 bit carry lookahead adder.5

4-bit Carry Lookahead Adder

A **4-bit Carry Lookahead Adder (CLA)** improves the speed of binary addition by reducing the carry propagation delay through the use of generate (G) and propagate (P) signals.

Structure:

1. Inputs:
   - Two 4-bit binary numbers: $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$
   - A carry input C_0.
2. Outputs:
   - 4-bit sum $S = S_3S_2S_1S_0$
   - Carry outputs C_1, C_2, C_3, C_4.

Generate and Propagate Signals:

- Generate (G): $G_i = A_i \cdot B_i$
- Propagate (P): $P_i = A_i + B_i$

Carry Calculation:

The carry signals are calculated as follows:

- $C_1 = G_0 + P_0 \cdot C_0$
- $C_2 = G_1 + P_1 \cdot C_1$
- $C_3 = G_2 + P_2 \cdot C_2$
- $C_4 = G_3 + P_3 \cdot C_3$

Sum Calculation:

The sum bits are calculated using the carry signals:

- $S_0 = P_0 \oplus C_0$
- $S_1 = P_1 \oplus C_1$
- $S_2 = P_2 \oplus C_2$
- $S_3 = P_3 \oplus C_3$

Summary:

- **The carry lookahead adder uses generate and propagate signals to quickly compute carry outputs, reducing the overall delay compared to traditional ripple-carry adders. This allows for faster addition in digital circuits.**

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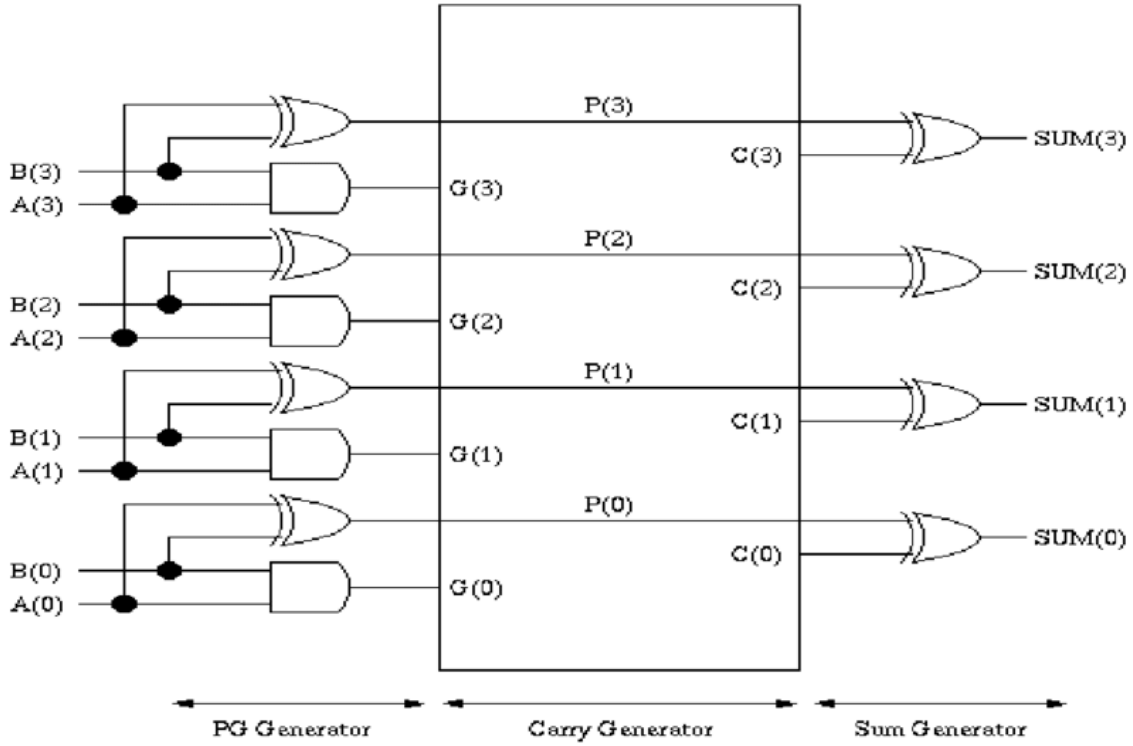

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3) Implement using CMOS lo0gic 1) 1-Bit full adder 2) DFF using TG. [10]

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5) state and explain different type of ROM memory

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6) Explain significance of clock gemneration in VLSI ddesign5

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7) Implement 3×3 array multiplier. 5

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Module 6

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1) a Illustrate RTL design of 3 TAP Serial FIR filter with HLSM,FSM and datapath. Calculate hardware required for 100 TAP filter.10

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3) Draw hlsm dispenser of Soda machine. 5

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